ABSTRACT

Signals sent from detectors through input units are inputted to a plurality of microcomputers, respectively. A plurality of microcomputers are synchronized with each other by external clock generating means provided commonly thereto, and executes an input processing and an arithmetic operation processing. In addition, a common memory provided as common storage means is connected to each of the plurality of microcomputers, which read out/write data from/to the common memory through respective buses. In such a manner, each of the plurality of microcomputers adopts a simple hardware configuration having the external clock and the common memory which are common to the plurality of microcomputers.